

REMARKS

Reconsideration of this application as amended is respectfully requested. Claim 8 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. Claims 1-8 and 10-15 are rejected under 35 § U.S.C. 102 (e) as being anticipated by U.S. patent number 6,535,939 by Arimilli et al. (hereinafter "Arimilli"). Claim 9 stands rejected under 35 U.S.C. § 103 (a) as being unpatentable over Arimilli in view of U.S. patent number 6,321,269 by Walker.

Claims 1, 3, 4, and 11 have been amended.

The Examiner has rejected claim 8 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention. The Examiner has stated that "Claim 8 recites the limitation 'the group' in line 1. There is insufficient antecedent basis for this limitation in the claim." The language in claim 8 is drafted in the traditional Markush form and language used. The language of the traditional Markush form uses "the group." Please refer to MPEP 2173.05(h). Therefore, the Examiner's 35 U.S.C. § 112 second paragraph rejection is inappropriate because no ambiguity exists and the above rejection is overcome. Applicant requests that the Examiner withdraw the above rejection.

Claims 1-8 and 10-15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Arimilli. However, applicant respectfully asserts that claim 1, as amended, is not anticipated by Arimilli under 35 U.S.C. § 102(e). Claim 1 states:

1. A method, comprising:

manufacturing a processor having a flexible architecture to service a multiple processor platform as well as a different application platform, wherein the processor contains
a plurality of N-bit registers, wherein N-bit is any number,
an XN-bit register, wherein X is a whole number greater than one and acts as a multiplier on the value of N,
a multiplexer connected to each of the N-bit registers and the XN-bit register, and
an arbiter connected to the multiplexer to direct the multiplexer to route signals from the N-bit registers or a signal from the XN-bit register depending upon the platform to be serviced.

(emphasis added)

In contrast, Arimilli does not disclose a processor containing any kind of registers. Arimilli also does not disclose a processor containing a multiplexer. Arimilli also does not disclose a processor containing an arbiter connected to the multiplexer to direct the multiplexer to route signals from the N-bit registers or a signal from the XN-bit register depending upon the platform to be serviced. Arimilli is completely silent on the existence of a processor containing any of the above components. Therefore, Arimilli does not disclose each and every limitation of claim 1. As such, independent claim 1 is not anticipated by Arimilli under 35 U.S.C. § 102(e).

Given that claims 2 and 3 depend from and include the limitations of claim 1, applicant submits that claims 2 and 3 are not anticipated by Arimilli under 35 U.S.C. § 102(e).

Applicant respectfully asserts that claim 4, as amended, is not anticipated by Arimilli under 35 U.S.C. § 102(e). Independent claim 4, as amended, states:

4. An apparatus, comprising:
an arbiter linked to a first processor having a flexible architecture with a first port and a second port, wherein the first processor contains a multiplexer, a first bit register connected in a signal path of the first port and a second bit register connected in a signal path of the second port;
a point to point bus; and

a device, the first port connected to the device through the point to point bus, wherein the arbiter directs the multiplexer whether to route signals from the first bit register as well as from the second bit register.

(emphasis added)

In contrast, Arimilli does not disclose a processor containing any registers. Arimilli also does not disclose a processor containing a multiplexer. Arimilli also does not disclose an arbiter directing the multiplexer whether to route signals from the first bit register as well as from the second bit register. Arimilli is completely silent on the existence of a processor containing any of the above components. Therefore, Arimilli does not disclose each and every limitation of claim 4. As such, independent claim 4 is not anticipated by Arimilli under 35 U.S.C. § 102(e).

Given that claims 5-10 depend from and include the limitations of claim 4, applicant submits that claims 5-10 are not anticipated by Arimilli under 35 U.S.C. § 102(e).

Applicant respectfully asserts that independent claim 11, as amended, is not anticipated by Arimilli under 35 U.S.C. § 102(e). Claim 11 states:

11. A method, comprising:
communicating between a processor and a device through a point to point bus;
using a signal pathway internal to the processor during the communications between the processor and the device;
changing the signal pathway within the processor to optimize a connection for an application; and
linking input signals from two or more ports of the processor to combine into a single input signal from the device depending on the application configured by a user.

(emphasis added)

In contrast, Arimilli does not disclose linking input signals from two or more ports of the processor to combine into a single input signal. Arimilli is completely silent about

combining signals from two or more port into a single input signal. Further, Armilli does not disclose linking input signals from two or more ports depending on the application configured by the user. Arimilli discloses logic to allow a vendor/manufacturer to change the bandwidth between devices. Arimilli discloses:

In a static implementation of the invention, which represents a primary implementation, a chip manufacturer creates the chips with configurable buses and provides them to various data processing system vendors. The configurable buses may be set using pins located on the chips. These pins may be set to an "off" or "on" position representing allocation of an affiliated bus to memory or other processors respectively. Thus a pin in the "off" position may represent use of that bus for memory while the pin in the "on" position represents use of the bus for other processor connections. Only one pin may control a number of configurable buses, or alternatively, each configurable bus may have its own individual pin. The vendor selects the particular configuration desired and sets the pins during assembly of the data processing systems. (i.e., The vendor configures the buses prior to installing the chips in the vendor's data processing systems). Thus Compaq Computers may set the pins to effectuate a wider processor to processor bus, while IBM may set the pins to off to effectuate a wider memory bus. Another vendor may share the buses equally between the memory and the other processors. In this static representation, each vendor is thus able to select a specific topology of data processing system based on the bus configurations.

(Arimilli Col. 7, Lns. 10-34) (emphasis added)

However, if a user buys a machine from the vendor configured, for example, as a server and the user's desired application of that machine changes to a workstation, then the user has no alternative except to buy another machine or get this one reconfigured from the vendor to suit its current application.

Armilli does not disclose linking input signals from two or more ports depending on the application configured by the user. Therefore, Armilli does not disclose each and every limitation of claim 11. As such, independent claim 11 is not anticipated by Armilli under 35 U.S.C. § 102(e).

Given that claims 12-15 depend from and include the limitations of claim 11, applicant submits that claims 12-15 are not anticipated by Armilli under 35 U.S.C. § 102(e).

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Arimilli in view of Walker. Applicant respectfully asserts that claim 9 is not obvious in view of Arimilli and Walker under 35 U.S.C. § 103(a). Walker discloses a client server network implementing transaction based protocol such as TCP. (See Walker Abstract paragraph).

The office action has provided inadequate motivation to combine the cited references under 35 USC § 103(a). The motivational reason given to combine the Arimilli reference and Walker was "to expand communication to a network." (Office Action, p. 6). The office action cites no hints or suggestions in either reference that actually suggests the combination of these two references. Walker makes no suggestion that the disclosed transaction based protocol could be used in a processor architecture. Arimilli makes no suggestion that the disclosed processor could use a transaction based protocol. The reasoning provided does not make particular findings of fact as to why a person skilled in the art of processor design would find the suggestion to use a multi-layered protocol architecture for that processor by implementing a network protocol function taught by Arimilli and/or Walker. The applicant requests a specific citing of facts to establish a prima facie case of obviousness by a preponderance of the evidence under 35 USC § 103(a).

Furthermore, neither Arimilli nor Walker, individually or in combination, disclose each and every limitation of claim 1. As discussed above, Arimilli does not disclose a

processor containing any registers. Arimilli also does not disclose a processor containing a multiplexer. Arimilli also does not disclose an arbiter directing the multiplexer whether to route signals from the first bit register as well as from the second bit register. Similarly, Walker does not discuss an arbiter directing the multiplexer whether to route signals from the first bit register as well as from the second bit register.


As such, claim 4, as amended, is not obvious in view of Arimilli and Walker under 35 USC § 103(a). Given claim 9 depends from and includes the limitations of claim 4, applicant submits that claim 9 is not obvious in view of Arimilli and Walker under 35 U.S.C. § 103(a).

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. A petition for an extension of time is submitted with this amendment. An Information Disclosure Statement is also submitted with this amendment. Applicants reserve all rights with respect to the application of the doctrine equivalents. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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